

Please type a plus sign (+) inside this box → ☐

PTO/SB/05 (4/98)
Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

Attorney Docket No. 98A-1919
First Inventor or Application Identifier Frederick J. Kiko
Title IMPEDANCE BLOCKING FILTER CIRCUIT
Express Mail Label No.

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ * Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☒ Specification [Total Pages 33]
(preferred arrangement set forth below)
 - Descriptive title of the Invention
 - Cross References to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference to Microfiche Appendix
 - Background of the Invention
 - Brief Summary of the Invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claim(s)
 - Abstract of the Disclosure
3. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 3]
4. Oath or Declaration [Total Pages 2]
 - a. ☒ Newly executed (original or copy)
 - b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
 - i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

5. ☐ Microfiche Computer Program (Appendix)
6. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
 - a. ☐ Computer Readable Copy
 - b. ☐ Paper Copy (identical to computer copy)
 - c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ☒ Assignment Papers (cover sheet & document(s))
8. ☐ 37 C.F.R. § 3.73(b) Statement of Power of Attorney (when there is an assignee)
9. ☐ English Translation Document (if applicable)
10. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
11. ☐ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. ☒ * Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired (PTO/SB/09-12)
14. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)
15. ☐ Other: _____

* NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: _____
Prior application information: Examiner _____ Group / Art Unit: _____

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

☐ Customer Number or Bar Code Label _____ or ☒ Correspondence address below
(Insert Customer No. or Attach bar code label here)

Name	DAVIS CHIN, ESQ.				
	Law Offices of Davis Chin				
Address	209 S. LaSalle Street				
	Suite 410				
City	Chicago	State	IL	Zip Code	60604-1202
Country	U.S.A.	Telephone	312-726-6448	Fax	312-368-0034

Name (Print/Type)	DAVIS CHIN	Registration No. (Attorney/Agent)	26,854
Signature	<i>Davis Chin</i>	Date	Nov. 18, 1998

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

11/19/98

FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1.
These are the fees effective October 1, 1997.
Entity payments must be supported by a small entity statement,
otherwise large entity fees must be paid. See Forms PTO/SB/09-12.
See 37 C.F.R. §§ 1.27 and 1.28.

TOTAL AMOUNT OF PAYMENT (\$ 435.00

Complete if Known

Application Number
Filing Date
First Named Inventor Frederick J. Kiko
Examiner Name
Group / Art Unit
Attorney Docket No. 98A-1919

METHOD OF PAYMENT (check one)

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number
Deposit Account Name

☐ Charge Any Additional Fee Required Under 37 C.F.R. §§ 1.16 and 1.17
☐ Charge the Issue Fee Set in 37 C.F.R. § 1.18 at the Mailing of the Notice of Allowance

2. ☒ Payment Enclosed:

☒ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
101 790	201 395	Utility filing fee	395.00
106 330	206 165	Design filing fee	
107 540	207 270	Plant filing fee	
108 790	208 395	Reissue filing fee	
114 150	214 75	Provisional filing fee	
SUBTOTAL (1)			(\$ 395.00)

2. EXTRA CLAIM FEES

Total Claims	Extra Claims	Fee from below	Fee Paid
20**	0	X	0.00
2	3**	0	0.00
Multiple Dependent			0.00

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
103 22	203 11	Claims in excess of 20	
102 82	202 41	Independent claims in excess of 3	
104 270	204 135	Multiple dependent claim, if not paid	
109 82	209 41	** Reissue independent claims over original patent	
110 22	210 11	** Reissue claims in excess of 20 and over original patent	
SUBTOTAL (2)			(\$ 00.00)

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
105 130	205 65	Surcharge - late filing fee or oath	
127 50	227 25	Surcharge - late provisional filing fee or cover sheet	
139 130	139 130	Non-English specification	
147 2,520	147 2,520	For filing a request for reexamination	
112 920*	112 920*	Requesting publication of SIR prior to Examiner action	
113 1,840*	113 1,840*	Requesting publication of SIR after Examiner action	
115 110	215 55	Extension for reply within first month	
116 400	216 200	Extension for reply within second month	
117 950	217 475	Extension for reply within third month	
118 1,510	218 755	Extension for reply within fourth month	
128 2,060	228 1,030	Extension for reply within fifth month	
119 310	219 155	Notice of Appeal	
120 310	220 155	Filing a brief in support of an appeal	
121 270	221 135	Request for oral hearing	
138 1,510	138 1,510	Petition to institute a public use proceeding	
140 110	240 55	Petition to revive - unavoidable	
141 1,320	241 660	Petition to revive - unintentional	
142 1,320	242 660	Utility issue fee (or reissue)	
143 450	243 225	Design issue fee	
144 670	244 335	Plant issue fee	
122 130	122 130	Petitions to the Commissioner	
123 50	123 50	Petitions related to provisional applications	
126 240	126 240	Submission of Information Disclosure Stmt	
581 40	581 40	Recording each patent assignment per property (times number of properties)	40.00
146 790	246 395	Filing a submission after final rejection (37 CFR 1.129(a))	
149 790	249 395	For each additional invention to be examined (37 CFR 1.129(b))	
Other fee (specify)			
Other fee (specify)			
SUBTOTAL (3)			(\$ 40.00)

* Reduced by Basic Filing Fee Paid

SUBMITTED BY

Typed or Printed Name DAVIS CHIN, Attorney of Record

Signature

Davis Chin

Date

11/16/98

Complete (if applicable)

Reg. Number

Deposit Account User ID

IMPEDANCE BLOCKING FILTER CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention:

5 This invention relates generally to telecommunication systems and more particularly, it relates to an impedance blocking filter circuit used in telecommunication systems for interconnecting between incoming telephone lines from a telephone company's central office
10 (C.O.) and subscriber or customer telephone equipment such as a telephone set located at a subscriber's premises so as to unconditionally block telephone impedance above 20 KHz.

2. Description of the Prior Art:

15 The prior art appears to be best exemplified in the following U.S. Letters Patent which were developed in a search directed to the subject matter in this application:

	4,613,732	4,823,383
20	4,742,541	5,642,416
	4,743,999	5,802,170

In U.S. Patent No. 4,823,383 issued to Cardot et al. on April 18, 1989, there is disclosed a protection device

for terminal equipment on telephone subscriber premises which includes a voltage surge protection circuit and/or a filter for providing protection against radio frequencies and interference. The filter is comprised
5 of series inductors **L1, L2, L3** and **L5** interconnected between terminals **E1** and **S1** and series inductors **L'1, L'2, L4** and **L'5** interconnected between terminals **E2** and **S2**. A capacitor **C5** is connected between the junctions of the inductors **L2, L3** and the inductors **L'2, L4**. The
10 surge protection circuit includes thermistors **TH1, TH2** and voltage limiters **D1-D3**.

In U.S. Patent No. 5,802,170 issued to Smith et al. on September 1, 1998, there is disclosed a customer bridge module for connecting telephone company wiring and
15 subscriber telephone wiring in a telephone network interface apparatus. In one embodiment, the customer bridge module includes overcurrent protection and an RFI filter. The overcurrent protection is formed by positive temperature coefficient resistors **220, 222** and inductors. The
20 RFI filter is formed by inductors **224a-224c, 226a-226c** and capacitors **236a-236c**. The inductors and capacitors are used to form a multi-pole low pass filter.

In U.S. Patent No. 5,642,416 issued to Hill et al. on June 24, 1997, there is disclosed an electromagnetic interference by-pass filter which suppresses RF noise currents conducted over the tip and ring leads of a telephone line-powered instrument. The filter includes first and second inductors **51, 53** and first and second capacitors **41, 43**.

It is generally well-known these days that many telephone subscribers or customers also have a personal computer located on their premises. At times, the computer user receives ADSL (an acronym for Asymmetric Digital Subscriber Line) signals from the Internet over the same telephone lines via an Internet Server Provider (ISP). In order to increase the speed of downloading of information from the Internet, an ADSL network interface is typically purchased and installed between the incoming telephone lines and the user's computer. However, since one or more telephone subscriber terminal equipment such as telephone sets, facsimile machines and/or answering devices are also connected to the same incoming telephone lines via internal house wiring, ADSL interference problems may be caused by the terminal equipment which can significantly limit or reduce the data rate. In one situation, it has been experienced that the change of

state from "on-hook" to "off-hook" of the telephone equipment and sometimes the telephone terminal equipment even being "on-hook" can create a resonance effect to occur so as to drop the impedance value to less than 10 Ω (Ohms) at a frequency as high as 500 KHz.

Accordingly, it would be desirable to provide an impedance blocking filter circuit for connection to the telephone terminal equipment causing the erratic input impedances. The impedance blocking filter circuit of the present invention is of a modular design so as to be easily connected in series with the offending telephone terminal equipment. The impedance blocking filter circuit blocks unconditionally any telephone impedances (e.g., open, short, capacitive, inductive, resonant, or any combination thereof) above the frequency of 20 KHz.

SUMMARY OF THE INVENTION

Accordingly, it is a general object of the present invention to provide an impedance blocking filter circuit which effectively and efficiently eliminates ADSL interference caused by telephone terminal equipment.

It is an object of the present invention to provide an impedance blocking filter circuit for connection to telephone terminal equipment causing the erratic input impedances.

5 It is another object of the present invention to provide an impedance blocking filter circuit used in telecommunication systems for interconnecting between incoming telephone line and customer's terminal equipment so as to unconditionally block impedance above 20 KHz due
10 to the customer's terminal equipment from an ADSL network interface unit and/or home networking interface unit.

It is still another object of the present invention to provide an impedance blocking filter circuit which is of a modular design so as to be easily connected in
15 series with the offending telephone terminal equipment.

It is still yet another object of the present invention to provide an impedance blocking filter circuit which is comprised of six inductors, two resistors, and a capacitor.

In accordance with a preferred embodiment of the present invention, there is provided an impedance blocking filter circuit used in telecommunication systems for interconnecting between incoming telephone lines and customer's terminal equipment so as to unconditionally block impedances above 20 KHz due to the customer's terminal equipment from an ADSL network interface unit and/or home networking interface unit. The filter circuit includes first, second and third inductors connected in series between a first input terminal and a first common point. The first inductor has its one end connected to the first input terminal and its other end connected to one end of the second inductor. The second inductor has its other end connected to one end of the third inductor. The third inductor has its other end connected to the first common point. A first resistor has its one end also connected to the first common point and its other end connected to a first output terminal.

The filter circuit further includes fourth, fifth and sixth inductors connected in series between a second input terminal and a second common point. The fourth inductor has its one end connected to the second input terminal and its other end connected to one end of the fifth inductor. The fifth inductor has its other end

connected to one end of the sixth inductor. The sixth inductor has its other end connected to the second common point. A second resistor has its one end also connected to the second common point and its other end connected to a second output terminal. A capacitor has its one end connected to the first common point and its other end connected to the second common point.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and advantages of the present invention will become more fully apparent from the following detailed description when read in conjunction with the accompanying drawings with like reference numerals indicating corresponding parts throughout, wherein:

Figure 1 is an overall block diagram of a telecommunication system for interconnecting a central office and a subscriber's premises, employing an impedance blocking filter circuit of the present invention;

Figure 2 is an exploded, perspective view of one form of a module housing the impedance blocking filter circuit;

Figure 3 is a schematic circuit diagram of an impedance blocking filter circuit, constructed in accordance with the principles of the present invention;

Figure 4 is a schematic circuit diagram of a second
5 embodiment of an impedance blocking filter circuit, in accordance with the principles of the present invention;

Figure 5 is a plot of input impedances of the impedance blocking filter circuit of Figure 3 for various telephone equipment impedances as a function of
10 frequency;

Figure 6 is a schematic circuit diagram of current limiting protection circuitry for use with the filter circuit of Figure 3; and

Figure 7 is a schematic circuit diagram of a home
15 network demarcation filter for use with the filter circuit of Figure 3.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now in detail to the drawings, there is illustrated in Figure 1 an overall block diagram of a

telecommunication system **10** for interconnecting a telephone company's central office (CO) **12** and a subscriber's premises **14** over a transmission media such as a conventional twisted pair of telephone lines **16**. The telecommunication system **10** employs a plurality of impedance blocking filter circuits, constructed in accordance with the principles of the present invention, in which each is contained in a modular housing **18**.

The central office **12** includes a telephone office switch **20** and an Internet Service Provider (ISP) **22**. The telephone office switch **20** is used to send voice signals via a low-pass filter **24** and a surge protector **26** to the telephone line **16**. The ISP **22** transmits ADSL data signals to a modem **28** which are then sent to the telephone lines **16** via a high-pass filter **30** and the surge protector **26**. It should be understood that the voice signals from the telephone office switch **20** and the ADSL data signals from the ISP **22** can be transmitted simultaneously to the telephone lines **16**. Further, the voice signals (speech) are in the frequency band between 300 and 3400 Hz, and the ADSL data signals are in the frequency band between 30 KHz and 2 MHz .

The subscriber's premises **14** includes a Network Interface Device (NID)/surge protector unit **32** which is connected to the incoming telephone lines **16** on its input side and is connected to the subscriber's internal wiring or house wiring **34** on its output side via a demarcation RJ-11 jack and plug unit **36**. As can be seen, the subscriber's premises further includes a number of terminal equipment such as a plurality of telephone sets **40**. At times, the computer user will be downloading information to a personal computer **38** from the Internet by receiving ADSL data signals transmitted by the ISP **22**.

In order to optimize the downloading of this information from the Internet, the user can purchase and install an ADSL network interface unit **42** for connection between the computer **38** and a RJ-11 jack and plug unit **44**. The ADSL network interface unit **42** includes a high-pass filter **41** connected to the RJ-11 unit **44** and an internal modem **43** connected to the computer **38**. The RJ-11 unit **44** is connected to the house wiring **34** for receiving the ADSL signals from the telephone lines **16**. However, it will be observed that the plurality of telephone sets **40** are also connected to the same house wiring **34** via RJ-11 units **46**, **48** and **50**, respectively.

If it were not for the impedance blocking filter circuits **18** in the present invention, the output impedance from each of the telephone sets **40** would be connected in parallel with the input impedance of the ADSL unit **42**. Since the output impedances from the telephone sets are subject to wide variations due to, for example, changing from "on-hook" to "off-hook" so as to present either an open, a short, capacitive, inductive, resonant, or any combination thereof at frequencies above 20 KHz, this erratic impedance can significantly affect the rate of the ADSL data signals being received by the computer **38** via the ADSL network interface unit **42**.

Therefore, the main purpose of the impedance blocking filter circuit of the present invention is to isolate the terminal equipment (telephone sets) impedances from the ADSL unit **42** and the house wiring **34** so as to eliminate degradation of the performance of the ADSL unit **42**. Further, the impedance blocking filter circuit serves to attenuate the ADSL data signal from being received by the telephone sets **40** in order to prevent non-linear conversion to voice band signals. Moreover, to facilitate the installation required by the customer, the filter circuit is contained in the modular housing **18**.

As can best be seen from Figure 2, one form of the modular housing **18** includes a base **52** and a snap-on removable cover **54**. The base has a printed circuit board **56** which is fixedly secured thereto by screws **58** and has
5 mounted thereon the electrical circuit components for the filter circuit **59**. One end of the modular housing **18** has a RJ-11 jack **60** formed integrally therewith for connection to the telephone set. This connection is achieved by plugging a RJ-11 plug (not shown) from a telephone set
10 into the jack **60**. The other end of the modular housing **18** has a short length of cable **62** extending therefrom and terminating in a RJ-11 plug **64** which is connectable to the house wiring. In particular, the plug **64** is connected to the house wiring **34** by plugging the same into
15 a wall socket (not shown) having a RJ-11 jack.

In Figure 3, there is shown a detailed schematic circuit diagram of the impedance blocking filter circuit **59** of the present invention for connection in series between the house wiring **34** and the terminal equipment
20 (telephone set) of Figure 1. The filter circuit **59** includes two input (tip and ring) terminals **66**, **68** which are connectable to the house wiring **34** via the RJ-11 plug **64** and two output (tip and ring) terminals **70**, **72** which are connectable to the telephone set **40** via the RJ-11

jack **60**. The filter circuit **59** is comprised of inductors **L1-L6**, a capacitor **C1**, and resistors **R1, R2**.

The inductors **L5, L3, L1** and the resistor **R1** are connected in series between the first or tip input terminal **66** and the first or tip output terminal **70**. Similarly, the inductors **L6, L4, L2** and the resistor **R2** are connected in series between the second or ring input terminal **68** and the second or ring output terminal **72**. The inductors **L5** and **L6** are each preferably formed of a ferrite toroid. The inductors **L3** and **L4** have the same inductance values, and the inductors **L1** and **L2** have the same inductance values. The inductor **L1** and the first resistor **R1** are connected together at a common point **A** and to one side of the capacitor **C1**. The inductor **L2** and the second resistor **R2** are connected together at a common point **B** and to the other side of the capacitor **C1**. The resistors **R1** and **R2** also have the same values.

As previously pointed out, the primary purpose of the impedance blocking filter circuit **59** is to block the impedances from the telephone set at above the frequency of 30 KHz from reaching the house wiring **34**, thereby preventing adverse performance of the ADSL network unit

42 (Figure 1). In particular, the ADSL data signals being in the frequency range of 30 KHz and 2 MHz are mainly blocked by the inductors **L1** and **L2**. However, it has been experienced that some telephone sets have an input capacitance of less than 5 nf which can cause resonant impedances to occur within the ADSL band. In order to eliminate this undesirable effect, the capacitor **C1** is used to lower any resonance into an acceptable dead band at around the 10 KHz frequency. Further, the capacitor **C1** also provides additional attenuation of the ADSL signals so as to prevent driving the telephone impedance into a non-linear region and converting the high frequency ADSL signals into audible signals which can be heard by the subscriber or converted to another ADSL band and cause ADSL interference. While there may still exist other minor resonances in the telephone set in the frequency range of between 20 KHz and 60 KHz, their undesirable effect is significantly reduced by the resistors **R1** and **R2** which produce a de-Q effect. It should be noted that the inductors **L1** and **L2** are formed as separate inductors so as to avoid longitudinal impedance problems as well as blocking differential impedances.

Since the inductors **L1** and **L2** have their own frequency limitations (e.g., self-resonant frequency), the inductors **L3** and **L4** are provided so as to block the telephone impedances in the frequency band of 1 MHz to 20 MHz. These inductors **L3**, **L4** are necessary when phoneline home networking interface units (Figure 1) are being used in conjunction with the ADSL network interface unit **42**, as will be explained hereinafter. The inductors **L5** and **L6** are provided so as to block the telephone set impedances in the frequency band of 20 MHz to 500 MHz, which will prevent any problems caused by TV/FM interference.

For completeness in the disclosure of the above-described filter circuit but not for purposes of limitation, the following representative values and component identifications are submitted. These values and components were employed in a filter circuit that was constructed and tested, and which provides high quality performance.

	<u>PART</u>	<u>TYPE or VALUE</u>
	L1, L2	10 mH
	L3, L4	220 μ H
	L5, L6	ferrite toroid, 75 μ H
	C1	20 nf
	R1, R2	22 Ω

With these above values being used, the input impedance of the impedance blocking filter circuit **59** was plotted for various telephone equipment impedances (e.g., open, short, capacitive, inductive, resonant, or a combination of these conditions) as a function of frequency and is illustrated in Figure 5. As can be seen from the various curves, the input impedance across the input terminals **66, 68** of the impedance blocking filter circuit **59** for any telephone impedances connected across its output terminals **70, 72** is equal to or greater than 2K Ohms at frequencies above 40 KHz.

The impedance blocking filter circuit **59** of Figure 3 is basically a second-order filter and has been found to minimize adequately voice band transmission effects when up to eight (8) filter circuits are installed into the telecommunication system of Figure 1. In order to provide higher attenuation at frequencies above 20 KHz, there is shown in Figure 4 a schematic circuit diagram of a second embodiment of a third-order impedance blocking filter circuit **59a** of the present invention. The third-order filter circuit of Figure 4 is substantially identical to the second-order filter circuit of Figure 3, except there has been added an inductor **L7** and an

inductor **L8**. The inductor **L7** is interconnected between the common point **A** and the first resistor **R1**, and the inductor **L8** is connected between the common point **B** and the second resistor **R2**. The inductors **L7** and **L8** have the same inductance values.

Based upon tests conducted on the third-order filter circuit of Figure 4, it was observed that higher attenuation was provided at frequencies above 20 KHz. However, it was found that the number of such third-order filter circuits which could be connected to the telecommunication system of Figure 1 was limited to three or four. This is due to the fact that the inductor values of **L1**, **L5**, **L7** and **L8** of Figure 4 are smaller (on the order of 5-10 mH) than the ones in Figure 3, the capacitor value of **C1** of Figure 4 is larger (on the order of 33-47 nf) than the one in Figure 3, and the additive capacitive loading caused by each added filter circuit will adversely affect the voice band performance. Thus, the optimized operation between voice performance and ADSL performance was found to exist when only three or four filter circuits **59a** were installed.

While the filter circuit of Figure 3 performed adequately, the inventor has found based upon further testing that a transient problem will occur when the telephone set goes "off-hook" at the peak of the ring signal.

5 This "off-hook" transient condition may cause current spikes to occur which are higher than 600 mA. As a result, the high current will tend to saturate the inductors, thereby momentarily lowering the input impedance of the filter circuit and thus adversely affects

10 the data on the ADSL signal being transmitted to the interface unit **42**.

In order to overcome this current transient problem, the inventors have developed fast current limiting protection circuitry **74** for providing protection against the

15 "off-hook" transients. In Figure 6 of the drawings, there is shown a schematic circuit diagram of the current limiting protection circuitry **74** which is comprised of depletion mode N-channel field-effect transistors (FET) **Q1, Q2**; resistors **R1a, R2a**; and varistors **RV1, RV2**. The

20 FET **Q1** has its drain electrode connected to a first input terminal **76**, its source electrode connected to one end of the resistor **R1a**, and its gate electrode connected to the other end of the resistor **R1a**. The common point **C** of the gate electrode of the transistor **Q1** and the resistor **R1a**

is also joined to the first output terminal **78**. Similarly, the FET **Q2** has its drain connected to a second input terminal **80**, its source connected to one end of the resistor **R2a**, and its gate electrode connected to the
5 other end of the resistor **R2a**. The common point **D** of the gate of the transistor **Q2** and the resistor **R2a** is also joined to a second output terminal **82**. One end of the varistor **RV1** is connected to the drain of the transistor **Q1**, and the other end thereof is connected to the common
10 point **C**. One end of the varistor **RV2** is connected to the drain of the transistor **Q2**, and the other end thereof is connected to the common point **D**.

In use, the current limiting protection circuitry **74** replaces the resistors **R1** and **R2** of Figure 3. The first
15 and second input terminals **76**, **80** of the protection circuitry **74** are connectable to the common points **A** and **B** of Figure 3, and the first and second output terminals **78**, **82** thereof are connected to the tip and ring output terminals **70**, **72** of Figure 3. The transistors **Q1**, **Q2** may
20 be similar to the ones commercially available from Supertex Corporation under their Part No. DN2530N3. The varistors may be similar to the type ZNR which are manufactured and sold by Panasonic Corporation. The resistors **R1a** and **R2a** have the same resistance value and

are on the order of 5-20 Ohms depending on the thresholds of the transistors **Q1, Q2**. It should be understood that the transistors **Q1, Q2** have a large tolerance on current limit and the resistors **R1a, R2a** permit the desired
5 current limit value to be adjusted. Alternatively, the resistors **R1a, R2a** may have a value of zero Ohms or be entirely eliminated.

In normal on-hook operation, the transistors **Q1** and **Q2** are rendered conductive and have an on-resistance
10 value of about 10 Ohms. When the telephone set goes "off-hook" into high ringing voltage, the gate-to-source voltage of the forward conducting FET will become more negative due to the resistors **R1a, R2a**. As a result, the resistance of the transistors **Q1, Q2** will go very high
15 which will limit the current spikes to approximately 70-100 mA. The transistor **Q1** serves to limit the current flowing in a first direction, and the transistor **Q2** serves to limit the current flow in a reverse direction. Further, the varistors **RV1, RV2** defining transient
20 protection means function to clamp transients caused by lightning and power shorts from damaging or destroying the FETs **Q1, Q2**.

In view of continuing increased use of home computers and the high demand for accessing of information from the Internet in the last decade or so, many of the subscribers will be multi-PC homes. As shown
5 in Figure 1, the subscriber's premises or small business will typically have a second computer **38a** also connected to the same internal house wiring **34**. In order to effect high-speed data transfer in the multi-PC environment, there will be required phoneline home networking
10 interface units **42a** for using the internal house wiring in the frequency band above 5 MHz so as to interconnect the multiple computers **38**, **38a** or other devices at data rates above 10 MB/s as illustrated. While the impedance filter circuit of the present invention adequately
15 filters and blocks the telephone impedances from the home networking signals, which are in the frequency band of 5-10 MHz, it will be noted that the home networking signals from the telephone company's C.O. are however still connected to the house wiring via the NID/surge protector
20 unit **32**.

In order to solve this problem, the inventor has developed a home network demarcation filter **84** as shown in dotted lines in Figure 1 for connection at a point of demarcation (NID/surge protector unit **32**) between the

telephone company's incoming lines **16** and the subscriber's internal house wiring **34** via the demarcation unit **36**. A schematic circuit diagram of the home network demarcation network is depicted in Figure 7. The

5 demarcation filter **84** includes two input (tip and ring) terminals **86, 88** which are connectable to the incoming lines via the jack side of the demarcation unit **36** in the NID/surge protector unit **32** and two output (tip and ring) terminals **90, 92** which are connectable to the internal

10 house wiring via the plug side of the demarcation unit **36**. The demarcation filter is comprised of six inductors **L9-L14** and two capacitors **C2, C3**. In use, the demarcation filter is transparent to the ADSL data signals having the frequencies between 30 KHz and 2 MHz

15 but will produce an attenuation of more than 40 dB for frequencies above 5 MHz. The demarcation filter will also provide an inductive input impedance for above 5 MHz frequency band so as to prevent loading down the home networking signals on the incoming phone lines and also

20 adds data security benefits.

From the foregoing detailed description, it can thus be seen that the present invention provides an impedance blocking filter circuit used in telecommunication systems for interconnecting between incoming telephone lines and

customer's terminal equipment so as to unconditionally
block impedances above 20 KHz due to the customer's
terminal equipment from an ADSL network interface unit
and/or home networking interface unit. The impedance
5 blocking filter circuit is comprised of six inductors,
two resistors, and a capacitor.

While there has been illustrated and described what
is at present considered to be a preferred embodiment of
the present invention, it will be understood by those
10 skilled in the art that various changes and modifications
may be made, and equivalents may be substituted for
elements thereof without departing from the true scope of
the invention. In addition, many modifications may be
made to adapt a particular situation or material to the
15 teachings of the invention without departing from the
central scope thereof. Therefore, it is intended that
this invention not be limited to the particular embodi-
ment disclosed as the best mode contemplated for carrying
out the invention, but that the invention will include
20 all embodiments falling within the scope of the appended
claims.

CLAIMS

1. An impedance blocking filter circuit used in telecommunication systems for interconnecting between incoming telephone lines and customer's terminal equipment so as to unconditionally block impedances from above 20 KHz due to the customer's terminal equipment from an ADSL network unit and/or home networking interface unit, said filter circuit comprising:

first, second, and third inductors connected in series between a first input terminal and a first common point;

said first inductor having its one end connected to said first input terminal and its other end connected to one end of said second inductor, said second inductor having its other end connected to one end of said third inductor, said third inductor having its other end connected to said first common point;

a first resistor having its one end also connected to said first common point and its other end connected to a first output terminal;

fourth, fifth, and sixth inductors
connected in series between a second input
25 terminal and a second common point;

said four inductor having its one end
connected to said second input terminal and
its other end connected to one end of said
fifth inductor, said fifth inductor having its
30 other end connected to one end of said sixth
inductor, said sixth inductor having its other
end connected to said second common point;

a second resistor having its one end also
connected to said second common point and its
35 other end connected to a second output
terminal; and

a capacitor having its one end connected
to said first common point and its other end
connected to said second common point.

2. An impedance blocking filter circuit as claimed
in Claim 1, wherein said first and fourth inductors are
comprised of ferrite toroids.

3. An impedance blocking filter circuit as claimed in Claim 2, wherein said second and fifth inductors have values on the order of 220 μ H.

4. An impedance blocking filter circuit as claimed in Claim 3, wherein said third and sixth inductors have values on the order of 10 mH.

5. An impedance blocking filter circuit as claimed in Claim 4, wherein said first and second resistors have values on the order of 22 Ohms.

6. An impedance blocking filter circuit as claimed in Claim 5, wherein said capacitor has the value on the order of 22 nf.

7. An impedance blocking filter circuit as claimed in Claim 1, further comprising current limiting protection means connected between said common points and said output terminals for reducing current spikes caused by the customer's terminal equipment going off-hook.

8. An impedance blocking filter circuit as claimed
in Claim 7, wherein said current limiting protection
means is comprised of first and second depletion mode
field-effect transistors and first and second transient
5 protection varistors.

9. An impedance blocking filter circuit as claimed
in Claim 8, wherein said first depletion mode field-
effect transistor has its conduction path electrodes
interconnected between said first common point and said
5 one end of said first resistor and its gate electrode
connected to said other end of said first resistor, said
second depletion mode field-effect transistor having its
conduction path electrodes interconnected between said
second common point and said one end of said second
10 resistor and its gate electrode connected to said other
end of said second resistor, said first varistor having
its one end connected also to said first common point and
its other end connected to said first output terminal,
said second varistor having its one end connected also to
15 said second common point and its other end connected to
said second output terminal.

10. An impedance blocking filter circuit used in telecommunication systems for interconnecting between incoming telephone lines and customer's terminal equipment so as to unconditionally block impedances from
5 above 20 KHz due to the customer's terminal equipment from an ADSL network unit and/or home networking interface unit, said filter circuit comprising:

first, second, and third inductors connected in series between a first input
10 terminal and a first common point;

said first inductor having its one end connected to said first input terminal and its other end connected to one end of said second inductor, said second inductor having its
15 other end connected to one end of said third inductor, said third inductor having its other end connected to said first common point;

a seventh inductor and a first resistor connected in series between said first common
20 point and a first output terminal, said seventh inductor having its one end connected also to said first common point and its other end connected to one end of said first

25 resistor, said first resistor having its other
end connected to a first output terminal;

fourth, fifth, and sixth inductors
connected in series between a second input
terminal and a second common point;

30 said fourth inductor having its one end
connected to said second input terminal and
its other end connected to one end of said
fifth inductor, said fifth inductor having its
other end connected to one end of said sixth
inductor, said sixth inductor having its other
35 end connected to said second common point;

40 an eighth inductor and a second resistor
connected in series between said second common
point and a second output terminal, said
eighth inductor having its one end connected
also to said second common point and its other
end connected to one end of said second
resistor, said second resistor having its
other end connected to a second output
terminal; and

45 a capacitor having its one end connected
to said first common point and its other end
connected to said second common point.

11. An impedance blocking filter circuit as claimed
in Claim 10, wherein said first and fourth inductors are
comprised of ferrite toroids.

12. An impedance blocking filter circuit as claimed
in Claim 11, wherein said second and fifth inductors have
values on the order of 220 μ H.

13. An impedance blocking filter circuit as claimed
in Claim 12, wherein said third and sixth inductors have
values on the order of 5-10 mH.

14. An impedance blocking filter circuit as claimed
in Claim 13, wherein said seventh and eighth inductors
have values on the order of 5-10 mH.

15. An impedance blocking filter circuit as claimed in Claim 14, wherein said first and second resistors have values on the order of 22 Ohms.

16. An impedance blocking filter circuit as claimed in Claim 15, wherein said capacitor has the value on the order of 47 nf.

17. An impedance blocking filter circuit as claimed in Claim 1, further comprising home network demarcation filter means interconnected between the incoming telephone lines and internal house wiring for blocking
5 the impedance of the customer's terminal equipment from home networking signals.

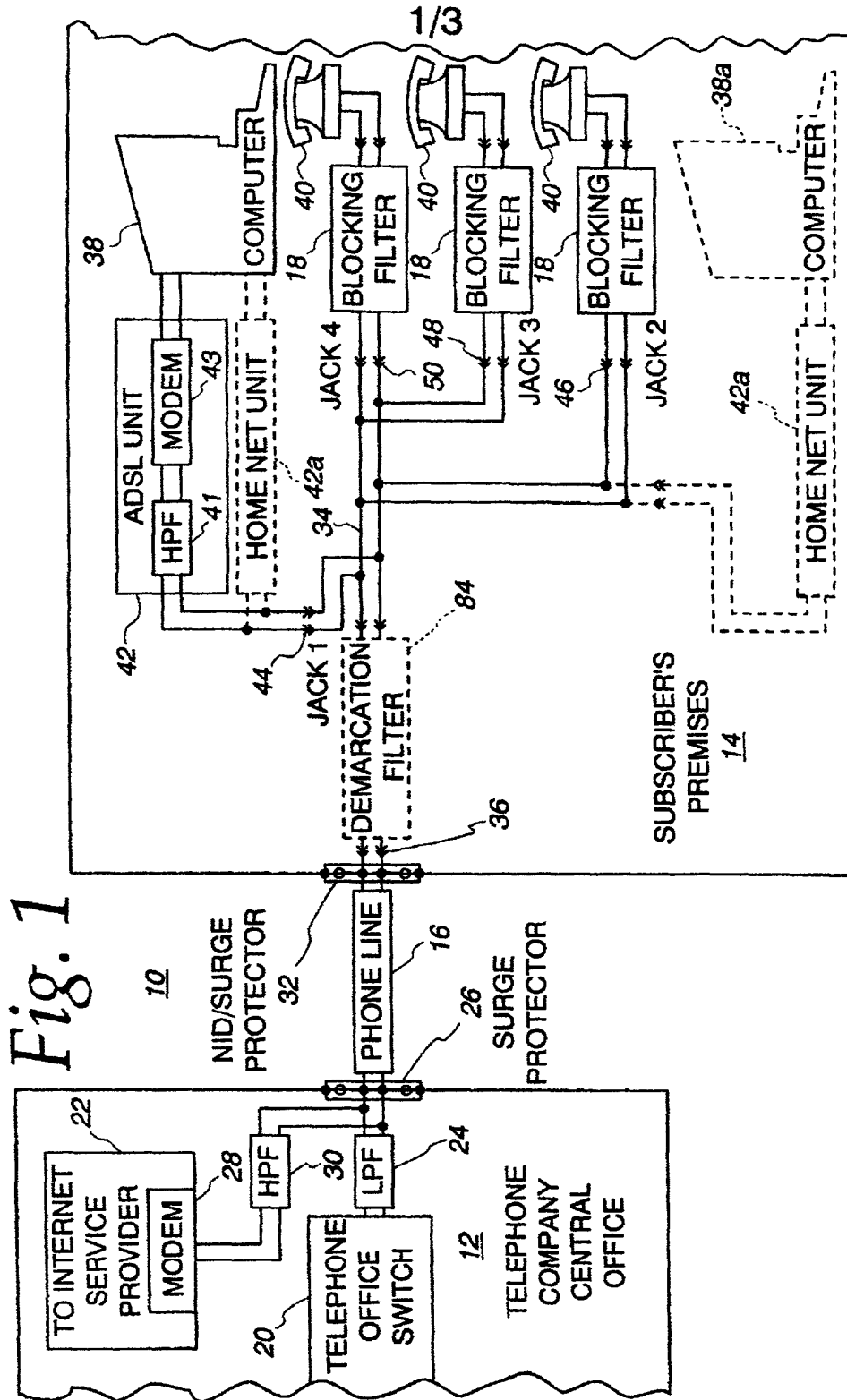
18. An impedance blocking filter circuit as claimed in Claim 17, said demarcation filter means is comprised of six inductors and two capacitors.

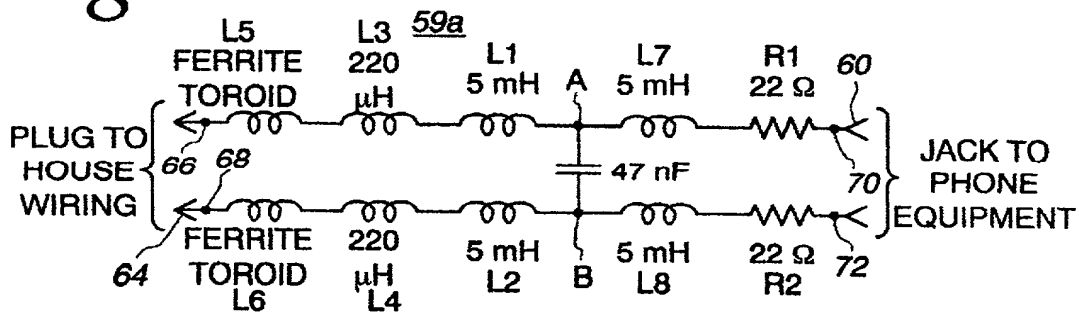
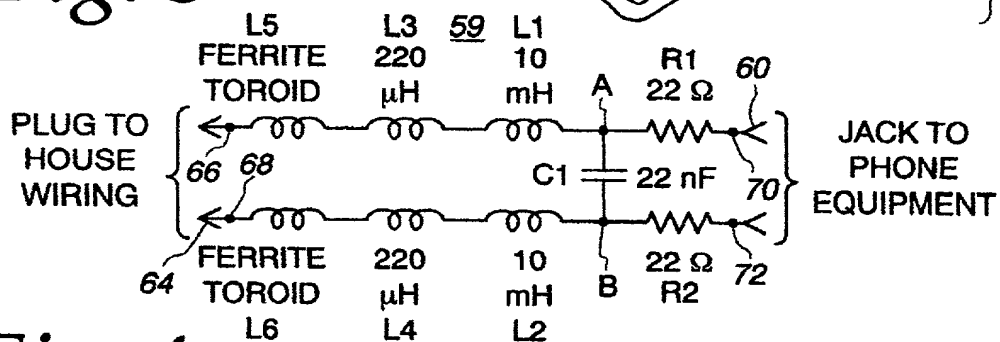
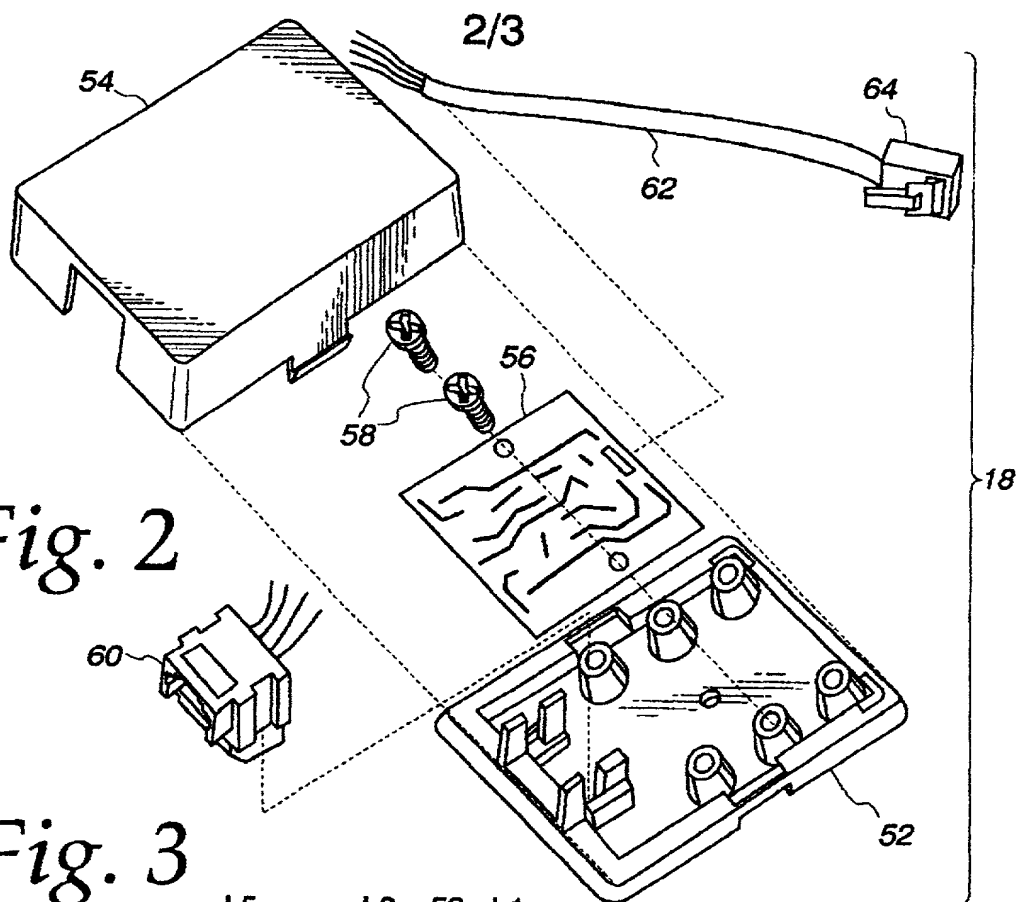
19. An impedance blocking filter circuit as claimed in Claim 10, further comprising home network demarcation filter means interconnected between the incoming

ABSTRACT OF THE DISCLOSURE

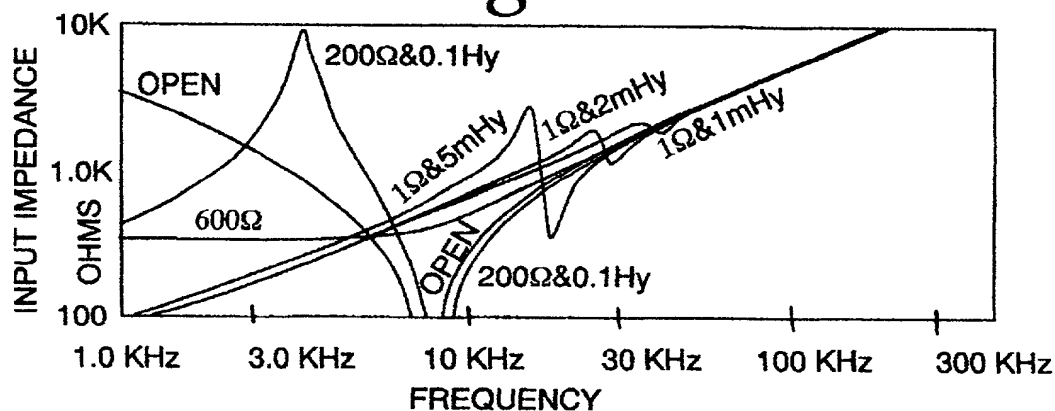
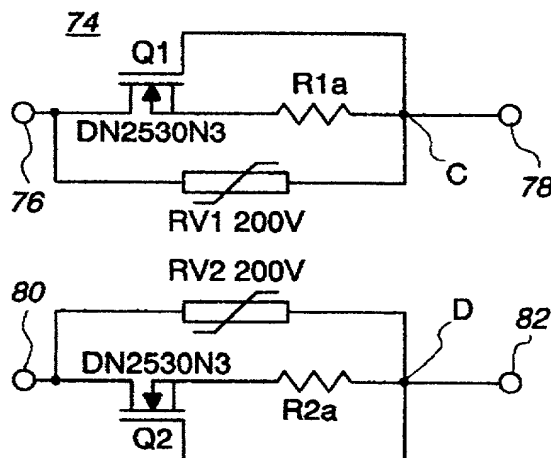
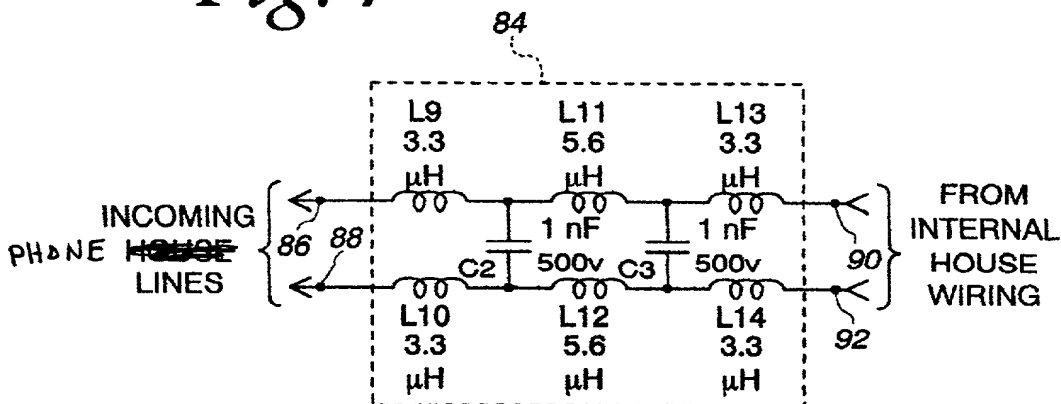
An impedance blocking filter circuit is provided for use in telecommunication systems for interconnecting between incoming telephone lines and customer's terminal equipment so as to unconditionally block impedances above 20 KHz due to the customer's terminal equipment from an ADSL network unit and/or home networking interface unit. The filter circuit includes first, second, and third inductors connected in series between a first input terminal and a first common point. A first resistor has its one end connected also to the first common point and its other end connected to a first output terminal. Fourth, fifth and sixth inductors are connected in series between a second input terminal and a second common point. A second resistor has its one end also connected to the second common point and its other end connected to a second output terminal. A capacitor has its ends connected across the first and second common points. In another aspect, the filter circuit also includes current limiting protection circuitry for reducing ring trip, dial pulse and off-hook transient current spikes.

Patented





3/3

Fig. 5*Fig. 6**Fig. 7*

Please type a plus sign (+) inside this box → ☐

PTO/SB/01 (12-97)

Approved for use through 9/30/00. OMB 0651-0032

Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

**DECLARATION FOR UTILITY OR
DESIGN
PATENT APPLICATION
(37 CFR 1.63)**

☒ Declaration Submitted with Initial Filing **OR** ☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number

98A-1919

First Named Inventor

Frederick J. Kiko

COMPLETE IF KNOWN

Application Number

/

Filing Date

Group Art Unit

Examiner Name

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

IMPEDANCE BLOCKING FILTER CIRCUIT

the specification of which

(Title of the Invention)

☒ is attached hereto
OR

☐ was filed on (MM/DD/YYYY) as United States Application Number or PCT International

Application Number and was amended on (MM/DD/YYYY) (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
				YES	NO
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)	<input type="checkbox"/> Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

[Page 1 of 2]

Burden Hour Statement: This form is estimated to take 0.4 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Please type a plus sign (+) inside this box → ☐

PTO/SB/01 (12-97)

Approved for use through 9/30/00. OMB 0651-0032

Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

DECLARATION — Utility or Design Patent Application

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

☐ Customer Number

OR

☒ Registered practitioner(s) name/registration number listed below

Place Customer
Number Bar Code
Label here

Name	Registration Number	Name	Registration Number
DAVIS CHIN	26,854		

☒ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto.

Direct all correspondence to: ☐ Customer Number or Bar Code Label

OR ☒ Correspondence address below


Name	DAVIS CHIN, ESQ., Attorney at Law				
Address	209 So. LaSalle Street				
Address	Suite 410				
City	Chicago	State	IL	ZIP	60604-1202
Country	USA	Telephone	312-726-6448	Fax	312-368-0034

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor:

☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
Frederick J.	Kiko

Inventor's Signature				Date	10/13/98		
Residence: City	Carlsbad	State	CA	Country	USA	Citizenship	USA
Post Office Address	3561 Donna Dr.						
Post Office Address							
City	Carlsbad	State	CA	ZIP	92008	Country	USA

☐ Additional inventors are being named on the _____ supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto

Applicant or Patentee: Frederick J. Kiko Attorney Docket
Serial or Patent No.: _____ No. 98A-1919
Filed or Issued: _____
For: IMPEDANCE BLOCKING FILTER CIRCUIT

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) AND 1.27(b)) - INDEPENDENT INVENTOR

As a below named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, to the Patent and Trademark Office with regard to the invention entitled IMPEDANCE BLOCKING FILTER CIRCUIT described in

- ☒ the specification filed herewith
☐ application Serial No. _____, filed _____
☐ Patent No. _____, issued _____

I have not assigned, granted, conveyed or licensed and am under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who could not be classified as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

- ☐ no such person, concern, or organization
☒ persons, concerns or organizations listed below*

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

FULL NAME Excelsus Technologies, Inc.
ADDRESS 3561 Donna Drive, Carlsbad, CA 92008
☐ INDIVIDUAL ☒ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

FULL NAME _____
ADDRESS _____
☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

FULL NAME _____
ADDRESS _____
☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Frederick J. Kiko
NAME OF INVENTOR NAME OF INVENTOR NAME OF INVENTOR

Signature of Inventor Signature of Inventor Signature of Inventor
Frederick J. Kiko
Date Date Date

✓ Nov 13 1998

Applicant or Patentee: Frederick J. Kiko Attorney Docket
Serial or Patent No.: _____ No. 98A-1919
Filed or Issued: _____
For: IMPEDANCE BLOCKING FILTER CIRCUIT

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) AND 1.27(c)) - SMALL BUSINESS CONCERN

I hereby declare that I am

- ☐ the owner of the small business concern identified below:
☒ an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN Excelsus Technologies, Inc.
ADDRESS OF CONCERN 3561 Donna Drive, Carlsbad, CA 92008

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled

IMPEDANCE BLOCKING FILTER CIRCUIT
by inventor(s) Frederick J. Kiko
described in

- ☒ the specification filed herewith
☐ application Serial No. _____, filed _____
☐ Patent No. _____, issued _____

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e). *NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

NAME NONE
ADDRESS _____
☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

NAME _____
ADDRESS _____
☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING Frederick J. Kiko
TITLE OF PERSON OTHER THAN OWNER President
ADDRESS OF PERSON SIGNING 3561 Donna Drive, Carlsbad, CA 92008

SIGNATURE

Frederick J. Kiko

DATE

NOV 13 1998